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(TITLE OF THE INVENTION)

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

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(CLAIMS)

1. A resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising:

inner leads having the thickness less than that of the lead frame blank; and

15 terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond a resin encapsulate, each inner lead

20 having a rectangular cross-section and having four

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surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using
10 a lead frame which is shaped in accordance with a two-step
etching process to a body wherein a thickness of inner
leads is less than that of the lead frame blank,
comprising:

15 inner leads having the thickness less than that of the
lead frame blank; and
20 terminal columns integrally connected to the inner
leads and having the same thickness with the lead frame
blank, the terminal columns possessing a column-shaped
configuration which is adapted to be electrically connected
to an external circuit, the terminal columns being disposed
outside of the inner leads in a manner such that they are
coupled to the inner leads in a direction orthogonal to the
thickness-wise direction thereof, portions of top ends of
25 the terminal columns being exposed to the outside beyond a
resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

10 3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

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4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

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5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

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6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads.

(DETAILED DESCRIPTION OF THE INVENTION)

(FIELD OF THE INVENTION)

15 The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

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(DESCRIPTION OF THE PRIOR ART)

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated 25 semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1513 to be electrically connected to the associated circuits, inner leads 1512 formed integrally with the outer leads 1513, bonding wires 1530 for electrically connecting the 5 tips of the inner leads 1512 to the bonding pad 1521 of the semiconductor chip 1520, and a resin 1540 encapsulating the semiconductor chip 1520 to protect the semiconductor chip 1520 from external stresses and contaminants. This resin- 10 encapsulated semiconductor device, after mounting the semiconductor chip 1520 on the bonding pad 1521, is manufactured by encapsulating the semiconductor chip 1520 with the resin. In this resin-encapsulated semiconductor device, the number of the inner leads 1512 is equal to that of the bonding pads 1521 of the semiconductor chip 1520. 15 And, FIG. 15(b) shows the configuration of a monolayer lead frame used as an assembly member of the resin-encapsulated semiconductor device shown in FIG. 15a. Such a lead frame includes the bonding pad 1521 for mounting the semiconductor chip, the inner leads 1512 to be electrically 20 connected to the semiconductor chip, the outer lead 1513 which is integral with the inner leads 1512 and is to be electrically connected to the associated circuits. This also includes dam bars 1514 serving as a dam when 25 encapsulating the semiconductor chip with the resin, and a frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy(a 42% Ni-Fe alloy), copper-based alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the 5 line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the 10 increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, 15 particularly quad plate package(QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small 20 pitches among lead frames for semiconductor packages are fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for 25 forming semiconductor packages having a large number of

Pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1420 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 14(d).

Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100 μ of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80 μ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.5 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged at pitches in the range of 0.13 to 0.16 mm, far smaller than 0.165 mm. When a lead frame is fabricated by processing a thin sheet of a reduced thickness, the strength of the outer leads of such a lead frame is not large enough to withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine leads arranged at very small pitches by etching.

An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half-etching or pressing to form the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

15 (SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals.

and resolving problems which are caused in assoc:
position shift and coplanarity of an outer lead.

(MEANS FOR SOLVING THE SUBJECT MATTERS)

5 According to one aspect of the present invention there is provided a resin-encapsulated semiconductor using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of the inner leads is less than that of the lead frame blank; and terminal columns comprising inner leads having the thickness less 10 of the lead frame blank; and terminal columns 15 connected to the inner leads and having the same thickness as the lead frame blank, the terminal columns being disposed in a column-shaped configuration which is adapted 20 electrically connected to an external circuit, the columns being disposed outside of the inner lead frame in a manner such that they are coupled to the inner lead frame in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions 25 arranged on top ends thereof, the terminal portions being made of solder, etc. and exposed to the outside being resin encapsulated, outer surfaces of the terminal columns also being exposed to the outside beyond the encapsulate, each inner lead possessing a rectangular cross-section and having four surfaces including a

surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns integral with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

20 [WORKING FUNCTIONS]

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the 25 forming process of the outer leads as in the case of using

20 a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the 10 semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the 15 first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

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[EMBODIMENTS]

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, 25 a resin-encapsulated semiconductor device in accordance

with a first embodiment of the present invention described hereinafter with reference to FIGS. 1 to 3. FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional view of a terminal column taken along the line B1-B2 of FIG. 1(a). Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a view of the resin-encapsulated semiconductor device of FIG. 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In FIGS. 1 and 2, a drawing reference numeral 100 represents an encapsulated semiconductor device, 110 a semiconductor chip, 111 electrodes (pads), 120 wires, 130 a lead, 131 inner leads, 131Aa a first surface, 131Ab a second surface, 131Ac a third surface, 131Ad a fourth surface, 132 terminal columns, 133A terminal portions, 133B surfaces, 133S a top surface, 135 a die pad, and 136 a resin encapsulate.

In the resin-encapsulated semiconductor device according to the first embodiment, as shown in FIG. 1(a), the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 105 at the surface thereof which is opposed to the other surface thereof where the electrodes pads 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131A of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133A located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 1(a) is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40 μ m whereas the portions 5 of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which 10 is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, 15 as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed. 20

25 In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the inner leads 131 is long or not. The inner leads having the contour, as shown in FIG. 9(a), in which the tips of the inner leads 131 are separated one from another, are prepared by the etching process, and the inner leads are resin-encapsulated after mounting the semiconductor chip thereon as will be described later. However, where the inner leads 131 are long in their length and have a tendency for the generation of twisting therein, it is impossible to fabricate the lead frame by etching to have the contour as shown in FIG. 9(a). Therefore, after etching the lead frame in a state where the tips of the inner leads are fixed to the connecting portion 131B as shown in FIG. 9(c)(1), the inner leads 131 are fixed with the reinforcing tape 160 as shown in FIG. 9(c)(D). Then, the connecting portions 131B which are not necessary in the fabrication of the resin-encapsulated semiconductor device are removed by a press as shown in FIG. 9(c)(V), and a semiconductor device is then mounted on the lead frame.

Hereinafter, a method for the fabrication of the resin-encapsulated semiconductor device will now be described with reference to FIG. 8. First, the lead frame 130A, as shown in FIG. 9(a), which is shaped by the etching process as will be described later, is prepared such that the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131ab of the inner leads 131 are bonded with each other using wires 120 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press to form terminal columns 133 and also the side surfaces 133b of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby (FIG. 6(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However, persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.15 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a clamping process for fixing the lead frame. Thus, an area to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be' ferric chloride solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm². The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth h corresponding to $2/3$ of the thickness of the lead frame blank (FIG. II (a)).

5 Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in 10 this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the 15 resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Incotec Inc.) by a die coater to form an etch-resistant layer 1180 so as to fill up the first recesses 1150 and to 20 cover the resist pattern 1120A (FIG. II (c)).

25 It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that the etch-resistant layer 1180 be coated over the entir

portion of the surface formed with the first recesses and first opening 1130, as shown in FIG. 11(c), because it is difficult to coat the etch-resistant layer 1180 on the surface portion including the first recesses.

5 Although the etch-resistant layer 1180 wax employed in this embodiment is an alkali-soluble wax, any surface-resistant to the etching action of the etchant solution remaining somewhat soft during etching may be used.

10 For forming the etch-resistant layer 1180 is not limited to the above-mentioned wax, but may be a wax of a UV-set type. Since each first recess 1130 etched by the primary etching process at the surface formed with the pattern is adapted to form a desired shape of the inner lead to be filled up with the etch-resistant layer 1180, it is

15 further etched in the following secondary etching process. The etch-resistant layer 1180 also enhances the mechanical strength of the lead frame blank for the second etching process, thereby enabling the second etching process to be conducted while keeping a high accuracy. It is

20 possible to enable a second etchant solution to be sprayed at an increased spraying pressure, for example, 2.5 kg or above, in the secondary etching process. The increased spraying pressure promotes the progress of etching in direction of the thickness of the lead frame blank in

25 secondary etching process. Then, the lead frame blank

subjected to a secondary etching process. In this secondary etching process, the lead frame blank 1100 is etched at its surface formed with first recesses 1150, having a flat etched bottom surface, to completely 5 perforate the second recesses 1160, thereby forming the tips of inner leads 131A (FIG. 11(d)).

The bottom surface 1170 of each recess formed by the primary etching process is flat. However, both side surfaces of each recess positioned at opposite sides of the bottom surface 1170 have a concave shape depressed toward the inside of the inner lead. Then, the lead frame blank 10 is cleaned. After completion of the cleaning process, the etch-resistant layer 1180, and resist films (resist patterns 1120A and 1120B) are sequentially removed. Thus, 15 a lead frame 130A having a structure of FIG. 9(a) is obtained in which tips of the inner leads 131A are arranged at a fine pitch. The removal of the etch-resistant layer 1180 and resist films (resist patterns 1120A and 1120B) is achieved using a sodium hydroxide solution serving to 20 dissolve them.

The processes for manufacturing the lead frame as shown in FIG. 11, is to form by means of etching the lead frame having the tips of the inner leads used in this embodiment of the present invention, which have a thickness 25 less than that of the lead frame. Especially, the first

surfaces 131Aa of the tips of the inner leads as shown in FIG. 1, are flushed with one surfaces of remaining portions of the inner leads having the same thickness with the lead frame while being opposed to the second surfaces 131Ab, and the third and fourth surfaces are formed to have a concave shape which is depressed toward the inside of the inner leads. Where a semiconductor chip is mounted on the second surfaces 131Ab of the inner leads by means of bumps for an electrical connection therebetween, as in a semiconductor device according to a third embodiment as will be described hereinafter, an increased tolerance for the connection by bumps is obtained when the second surface 131Ab has a concave shape depressed toward the inside of the inner lead. To this end, an etching method shown in FIG. 12 is adopted in this case. The etching method shown in FIG. 12 is the same as that of FIG. 11 in association with its primary etching process. After completion of the primary etching process, the etching method is conducted in a manner different from that of the etching method of FIG. 11 in that the second etching process is conducted at the side of the first recesses 1150 after filling up the second recesses 1160 by the etch-resist layer 1180, thereby completely perforating the second recesses 1160. At this time, by implementing the primary etching process, etching at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131Ab, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness t of the inner lead tip which is finally obtained. For example, where the blank has a thickness t reduced to 50 μm , the inner leads can have a fineness corresponding to a lead width W_1 of 100 μm and a tip pitch p of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness t of about 30 μm and a lead

width W_1 of 70 μm , it is possible to form inner leads having a fineness corresponding to an inner lead pitch p of 0.12 mm. Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness t and the lead width W_1 . That is to say, an inner lead tip pitch p up to 0.08 mm, a blank thickness up to 25 μm , and a lead width W_1 up to 40 μm can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape) is generally used, as shown in FIG. 9(c)(a). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(b), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereto. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

10 The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width W_1 slightly greater than the width W_2 of an opposite surface. The widths W_1 and W_2 (about 1000 μ m) are more than the width W at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(2)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(B)(a), there has particularly excellent in wire-bonding property, because the etched flat surface does not have roughness. FIG. 13(B) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared to that of the etched flat surface of this first embodiment. FIG. 13(2) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(2). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(2)(a) or FIG. 13(2)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGS. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGS. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified

example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device, 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 270, and the semiconductor chip 210 is electrically connected at its 5 electrodes (pads) 211 to the second surfaces 231ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated 10 semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located 15 on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which 20 is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner 25 leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process 5 for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230, as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(□), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGS. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG. 25

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side 5 surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present 10 invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional 15 view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing 20 reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 330 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(1)(b), both widths W1A and W2A (about 100 μ m) at top and bottom ends of the inner leads 331 are larger than a width WA at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(0)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5 Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-
10 sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of this fourth embodiment is
15 substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing reference numeral 400 represents a semiconductor device, 410 a semiconductor chip, 411 pads, 430 a lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth embodiment, one surface of the semiconductor chip 410 on
20 which the pads 411 are disposed is fastened to the second
25 surface 431Ab of the inner lead 431.

surfaces 431Ab of the inner leads 431 by the insul.
5 adhesive 470, and the pads 411 and the first surfaces
of the inner leads 431 are electrically connected with
other by wires 420. The semiconductor device of
the fourth embodiment uses the same lead frame which is use
10 the third embodiment, which has the contour as shown
FIG. 10(a) and 10(b). Also, in the case of this fourth
embodiment, as in the case of the first and second
embodiments, the electrical connection between the res-
15 encapsulated semiconductor device 400 of this embodiment
and an external circuit is achieved by mounting the res-
encapsulated semiconductor device 400 via the terminal
portions 433A each being made of a semi-spherical solder
20 on a printed circuit substrate, with the terminal portion
433A located on the top surfaces of the terminal column
433, respectively.

FIG. 7(d) is a cross-sectional view illustrating
25 a modified example of the semiconductor device in accordance
with the fourth embodiment of the present invention. In the
modified example of the semiconductor device as shown
in FIG. 7(d), the terminal portions each comprising the
semi-spherical solder are not provided, and the top
surfaces of the terminal columns are directly used as the
terminal portions. Because the protective frame is not
25 used and the side surfaces 433B of the terminal columns 433

are exposed to the outside, a checking operation by a test, etc. can be easily performed.

(EFFECTS OF THE INVENTION)

5 The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this
10 invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem
15 associated with coplanarity. In addition to these advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay
20 time.

59:543 v1

59:543 v1

は大化が進んで、その結果、圧力測定部はこれまでにQFP (Quad Flat Package) 及びTQFP (Thin Quad Flat Package) など) までは、リードの多ピン化がさしかなってきた。上記のキヤノン電子用いられるリードフレームは、既存のものはオトトリソグラフィー技術を用いたニッティングは二万ビンによりますされ、既存でないものにプレスによる加工万ビンによる加工されるのが一般的であったが、このようなキヤノン電子の多ピン化にはい、リードフレームにおいても、インカーリード既存の表面化が違う。当社は、既存のものに対しては、プレスによる加工は止めよからず、リードフレーム底面の底面が0.25mmほどのものを用い、ニッティング加工で対応してきた。このニッティングは二万ビンの工法について以下、図14に基づいて概要に述べておく。先ず、底面をもしくはく2×ニッケル-銅合金からなる底面0.25mm程度の底面(リードフレームニズム1410)を十社底面(图14(c))したは、エクロヒビカリツムモダルスとした後底面デザインレジスト面のオオトレジスト1410とし、底面の底面に同一に生産する。(图14(d))次いで、既定のパターンが既成されたマスクを介して示圧着灯でレジスト面を露光したは、既定の露光部でエキア光レジストを露光して(图14(e))。レジストパターン1430を形成して、底面露光部の底面露光部をそぞろに元して行く。塩化第二鉄水溶液を三たらみ分とてちりニッティング底にて、スプレイにて露光底(リードフレームニズム1410)に吹き付ける既成の底面にニッティングし、干渉させる。(图14(f))。しないで、レジスト露光部を露光処理し(图14(g))。底面露光部のリードフレームを用いて、ニッティングニッケル底を形成する。このように、ニッティングニッケルによっては露を飛ばすリードフレームに、更に、既定のエリアに5mm×5mmが形成される。よいで、底面、底面の露を飛ばす、インカーリード部を露光用紙を用いてボリュミドテープにてテークリング処理したり、必要に応じて既定の露タブ用リバーを回り加工し、ダイバッド部をダクンセットする露を飛ばす。しかし、ニッティングニッティングは二万ビンにおいては、ニヤケンシング基によろ底面は既成二万ビンの第一ルートの地に底面(底)万ビンにも達したり、その表面化加工にも複数があるのが一般的で、图14に示すように、リードフレーム底面の底面からニッティングするため、ラインノード・スリーブ・ノードの底面を、ケイン部はがこよこよには、底面の50~100%程度とされている。又、リードフレームの底面は二万ビンのアワーリードの底面をもつた場合、一般的には、その底面は約0.125mm以上必要とされている。この点、图14に示すようなニッティングニッティングの底面の底面は約70~80μmを算出し、0.165mmビンチ底面の底面はインナー

リード式元請のエッティングによる丸ニギを正規してさうが、これが農民とされていた。

〔0.004〕しかしながら、既に、またはドリルニードルでは、小バッケージでは、まだ電子であるインテリードのピッチが0.165mmピッチを見て、既に0.15mmピッチまでの半ピッチ化をスケッチしておなじと、エッチング加工において、リード距離のままでなくした場合は、アセンブリ工場やマスク工場といった後工程におけるアフターリードの必要性が現じていながら、既にリード距離の距離をなくしてエッチング加工を行う方法にも努力が出てきた。

(00051) これに応応する方たとして、アカーリードの見本を提出したまま測定を行つた所で、インテリード部分をハーフニッティングもしくはプレスにより組んでニッティング加工を行う方たが提出されていました。しかし、プレスにより組んでエッティングが工をあこなう場合には、は工場においての用意が不足する(例えは、つうとエリアの不具合)。テクニカルにてモールチゼンのクランプに必要なインテリードの見本。アモリード部分が提出されない。完成を2段行なわなければならぬ場合は二種が用意が頂けになら、両端部が多くある。そして、インテリード部分をハーフニッティングにより組んでエッティング加工を行う方たの場合はにも、部端を2段行なわなければならず。製造工場が対応にならうといふのがあり、いざれも実用化には、まだ至っていないのが状況である。

00061) が最もじょうとするは毎に二万一千キロメートルの多
元化にはいインテリードビットが近くたらみ) には
多モススルう口に、アフターリードの位置ボレ(ス
ク) やモモタ(コブラナリティ) の位置をじかに
の高さとなってきた。ただしに、このような方式のも
多元化にかかって、且つ、アフターリードの位置
(スキュ) やモモタ(コブラナリティ) の位置
しかねでから多モススルの高さをしこすてらもので

1007】 1日を終めてたる日の午後7時頃の所感は止み難い。 2日はエッティング加工によりインテリードの一・ ハーフフレームミリの厚さよりし反面に丸み加工一 たりードフレームを用いたキヤロは堅苦であって、 ハードフレームとリードフレームとハーフフレームよりなるコンセー- テリードと、はインテリードに一例にぎはし- ードフレームとだと同じほどの力弱さと反対する のミリの厚さとをもし、且つ、ミリはインテリードの力弱さにおいてインテリードに付してはミリ は反してだけられており、ミリの先端はミリ三 ならミリをかけ、ミリをかけた風景は日からは二- 、ミリの力弱さのあたはミリに風景は日から出で たり、インテリードに、斯正良はが4万戸で声!

(付属) 工具類の取扱い方法を記述するに、上記のとおりに操作することにより、リードフレームを失いたい工具を止める方法において、多段化に加えて、且つ、各部の区分 (b) に示すとおりリードフレームを失いたい場合のように、アクリルートのオーミングニードルを工具としない場合、これらの工具に起因して発生していくアクリルードのスニーカーの原因やアクリルードの原因 (コアブレーティー) の問題を全く無くすることは不可能であることは既に既述の如く可なりとするのである。又しくは、2段エンシング加工によりインシーリードの工具がそれの原因よりも既に既述の如く加工された。又、インシーリードを既述に加工された多段のリードフレームを用いることにより、多段化の多段化に加えて工具としてのものとしている。更に、既述する、区分 (b) に示す2段エンシングにより既述されたリードフレームを用いることにより、インシーリード区分 (b) はモードを示す。ワイヤボンディングはのましのとしている。又 (1) 区はモードで、又 (2) 区はインシーリードモードである。又 (3) 区はインシーリード既に既述の如くモードである。又 (4) 区はインシーリード既に既述の如くモードである。又 (5) 区はインシーリード既に既述の如くモードである。

180を並げる必要なく、図1(d)に示すような左端180を並べない構造の三面鏡を用い、
[001]180。

100101 天井内)のニッケルは100に使用のサードフレーム130に、42Xニッケル-黄銅をニッケルとしたもので、そして、図9 (a) に示すような形状をした。エッチングにより内面加工されたリードフレーム130Aを示したもので、図9 (b) に示すように内面や他の部分の底面より天井に形成されたインナーリード部131をもつ。ダムバー136は高さが止まる底のダムとなる。図9 (c) に示すような形状をした。エッチングにより内面加工されたりードフレーム130を、天井内においては用いたが、インナーリード部131とチップ部133以外は実質的に不要なものであるから、この形状に限定はしない。インナーリード部131の底面には4.0 μm、インナーリード部131以外の底面には0.15 mmでリードフレーム底面の底面の底面の底面に0.5 mmに限らず天井に0.125 m~0.50 mmまででも良い。また、インナーリードピッチは0.12 mmと長いピッチで、ニッケル底面の多段化に拘束されないのとしている。インナーリード部131の底面131Aには平面上でワイヤボンディングしやすい形状とおり、図1 (b) に示すように、第3面131Aと第4面131A Cにはインナーリード側へ凹んだ形状であり、第2面131A b (ワイヤボンディングを良くしても実質的に良いものとしている。

0.1.1) エヌ局内においては、インテリード13号がどこかで、インテリード13号にミレが付下さい。及び図9(8)に示すような、インテード元気がそれぞれ個別された尼氏のリードフレームレジスト方式にして仕立てて、これらを複数する万台に及ぶ生タテをなくしておおむね止している。インテレミーが名く、インテリード13号にミレをいい場合には、図9(4)に示すればにニッヂ二つすることに出来ないため、図9(6)ト(イ)に、うにインテリード先端部を通常部131Bにては終端にニッティング加工したは、インテリード端部を再生チップ160で固定し、(図9(6)ト(イ))、おいてプレスにて、そのまま再生チップの間には通常部131Bを跨し、この位置でチップを主としてニッティング加工する。(図9(6))

21 次に支点内側の取付部止端をヨコエミの
モニタ8に沿つて周囲に旋削する。次に
チッピング加工にてカスを飛ばす。图9(1)に
ドフレーム130Aを、インアーリード130
2E131Aもが写真で上にならうようにして用
(图8(1))。

ました。 (図8 (b))
モダムモード110モダイバンド: 35にモダムモード
モダムモード110のモダムモード111とインテーリー。モ
1次電のス2区とモダイバンド: 20にてモダムモード
ました。 (図8 (c))

10 た。 (問 8 (c))
図 9 に示すリードフレーム: 300 μm のタップバー: 300
μm のリード: 100 μm を示した。これは、リードフレー
ムの端子部の内側の面にセロロイドの三日から四日で元
の形に復元して、セロロイドを剥離した。 (S 3
(c))

それで、最初に180を基準に190を介してステムの剛性を高めようように、車両全般に受けた。(88(1)) 例、ピボットなどには、車体重量の2倍の剛性、車体の剛性が高められることにより前部サスペンションとステムの剛性から車輪が入りこまねるまでにクラックが入りやすくなり、そういうことがないようにするふに受けたものであるが、必ずしも車としない。また、車方にによる車輪に歯車の型を用いて行うが、車体が2倍！10のティーズで、且つ、ノードカーブの車体の車輪の歯が車体を走がうれば車体へ飛出したばかりで止した。

ターン等を用いて、所定尺寸の第一の端口部1110
・第二の端口部1111をもつて、ハンドル部1112を
O.A. 111208を完成した。図11(4)
の端口部1110は、ほのニッテン加工において
ードフレーム24H1110とこの端口部からベタ状に
ードフレーム24Hよりしで端口部にするためのもの
レジストの第二の端口部11140は、インテーリー
モタルの名前を冠するためのものである。第一の端
1112012。少なくともリードフレーム1110の
リード先端部を端部をさしが、は工具において

て、テーピングの工場や、リードフレームを販売するクランチエ工場で、ベタ板に直接それを分別に置くようになった部分との位置が部品になる場合があらうので、ニッティングを行なうエリアはインテリード先端の又とか工区だけにして大きめにどう必要がある。次いで、底板57°C.、上部48ボーメの硝化第二鉛を用いて、スプレーは2.5kg/m²にて、レジストパターンが形成されたりードフレームは1110の上面をニッティングし、ベタ板(チタニウム)に直接された第一のビーム1150の上にそれがリードフレーム位置の約2/3程度に達した時にエッティングを止めた。(図11(b))

上記ス1回目のエッティングにおいては、リードフレーム
ヨリ1110の位置から同時にニッティングを行ったが、
必ずしも位置から同時にエッティングする必要はない。エ
ヌ死ガのように、ス1回目のエッティングにおいてリード
フレームヨリ1110の位置から同時にエッティングする
場合は、位置からエッティングするところにより、R-E-T-L
ス2回目のニッティング時間を見計らうため、レジスト
パターン920B側からのみの位置エッティングの場合と
にべ、ス1回目エッティングとス2回目エッティングのト
ータル時間が増加する。そこで、第一のヨリ1130
側の位置された第一の位置1500にニッティングを実施
1180としての前エッティングなどのうちホットメルトコ
ンクスス(ブレインクス元ニッケル電極の位置)を...22...
MR-WB6を、ダイコータモ皮で、こなし、ペタ
吹(平手吹)に位置された第一の位置1150に埋め込
んだ。レジストパターン1120以上も位置ニッティングを
実施1180に位置された位置とした。(图11
(c))

インテリードモスクワ31人を殺した。(S: (c))

ス1回目のニッティング本工にて作成された。リードフレーム面に示すニッティング本工には表示であらうが、この点をあし2点はインテリード机にへこんだ点である。ないで、次々、ニッティング表示を200の点でレジストロ（レジストロパターン1120A-1120S）の点を示す。インテリード表示201-201Aが2点表示された。図9（a）に示すリードフレーム1120Aを示す。ニッティング表示1120とレジストロ（レジストロパターン1120A、11280）の点は示す。リードフレーム本工はにより2点示した。

〔0014〕上記、図11に示すリードフレームの形状
万円に、又太さに用いられる。インナーリード先端部
を又同に加工したリードフレームをエッチング加工に
により造り下る万円で、图1に示す、インナーリード
先端の第1区1.3-1.1Aを又同形状の他の部分と同
様に、又2区1.3-1.1Aと同方向させて左折し、且つ、又
区1.3-1.1A、第4区1.3-1.1Aをインナーリードの
側に向かって凹んだ形にて下るエッチング加工万円で
ある。次に下る又区1.3-1.1Aのキズは底のようになシブを
いてキズを生じてモインナーリードの第2区1.3-1.1Aを
左折し、インナーリードと又底に接する場合に
又、第2区1.3-1.1Aをインナーリード側に凹んだ形にて
左折した方がパンプ形状の口の片合が大きくなる
。图12に示すエッチング加工万円が用いられる。图1
に示すエッチング加工万円は、第1回目のエッチング
度では、图11に示す万円と同様であるが、エッテ
ングが区1.1-1.0を第2の区1.1-1.0時に造る迄
は、第一の区1.1-1.0側から第2区1.1のエッチング
を行い、又造りこもて見なつていて、图11第1回目
エッチングにて、第二回目区1.1-1.0からのエッチン
グ充分に造っておく。图12に示すエッチング加工万円
によって造られたリードフレームのインナーリード先
端部の形状には、图6(b)に示すように、又2区1.3-
1.1がインナーリード側にへこんだM字形に造

方のうちに、エッティングを2段階にわけて行うエッティング加工方針を、一石には2段エッティング加工方針っており、又はエッティング加工方針であら、又はいた四九(ふ)に示す、リードフレームL130Aに付けては、2段エッティング加工方針、バクタスを工夫することにより部分的にリードフレームをよくしながらエッティングを行う方針とが併用してはらり、リードフレームL130Aを廻くした部分においては、通常な加工ができるようにしてはる。四九(ふ)に示す、上記の方針にないては、インナーリードフレームL131Aの外側加工は、第二の四四(一)はと、長尺的にはうらるインナーリードフレームの外側をカットする方針である。又は、第三の四四(二)

さて見てみると、図11(e)に示す、半径はW1を1.00mmとして、インナーリード丸み部ピッチ0.15mmまで粗加工可能となる。長さ15.00mmは区でなくし、半径W1を7.00mm程度とすると、インナーリード丸み部ピッチ0.12mm程度まで粗加工ができるが、粗加工し、半径W1のとり万次第でインナーリード丸み部ピッチ0.15mmに更に良いピッチまで粗加工可能となる。ちなみに、インナーリード丸み部ピッチ0.08mm、長さ25.00mmで半径は4.00mm半径が可能である。

〔0016〕このようにエッチング加工にてリードフレームを形成する。インナーリードの名前が覚かしい場合は、電気工場でインナーリードのヨレが発生しにくい場合には、後方図9(1)に示す形状のリードフレームエッチング加工にてはるが、インナーリードの名前が長く、インナーリードにヨレが発生しやすい場合には、図9(c) (イ)に示すように、インナーリード先端部から左右第131Bを抜け、イジアリード先端部を削除した形にしてあらしたものを用て、これは2次注塑時に不必多な遮蔽部131Bをアプレス等により削除して図9(4)に示す形状を用る。尚、前述のように、図9(c) (イ)に示すものも切断し、図9(4)に示す形状に下るには、図9(c) (ロ)に示すように、2次注塑のため遮蔽テープ1-6-0(ポリイミドテープ)を接着する。図9(c) (ロ)のは縦で、アプレス等により遮蔽部131Bを切断するが、遮蔽テープは、テープをつけた状態のままで、リードフレームに固定され、そのままで粘着止められる。後、エアーブラストにて遮蔽部分を示すものである。

の両面に平底ではあるが、この部分の底面をみて、
ペスをくどれない。また両面ともリードフレームに
てある。底面（ボンディング）面には表示記号、右に
チップエモーションよりある。図13（二）にアレス（ニー
シング）によりインナーリード先端部を露出させたま
まチップ加工によりインナーリード先端部：133：C
133 1 Dを加工したものの、ニコエニニ（表示マー
ク）との位置（ボンディング）を示したものであるが、こ
れにはアレス止めが底に示すように三方にぶつけて、

10 ため、どちらの筆を用いても可（ポンティング）して
6、6.111 (二) の (a)、(b) に示すように筆
(ポンティング) の間に空きが全く無く、或めにむかは
なう書きが多い。6. 1321 へりにニイニシグエア
3

(0018) 次に支点外の支点付近型と支点付近の支点外型を並げると、図3 (a)～図3 (c) は、それぞれ、
は支点外の支点付近型と支点付近の支点外の支点付近型で
ある。図3 (a) に示す支点外の支点付近型には、支点外
1の三はさみ型などは、ダイバッド1135の四角が含まれ
るもので、ダイバッド1135が内孔に固定している。ダ
イバッド1135が内孔に突出していることにより、支
点外1に比べ、他の穴孔が確保されている。図3 (b) に
示す支点外の支点付近型も、ダイバッド1135が内孔
1に突出させているものである。支点外1に比べ、他の穴
孔が確保されている。支点外1や図3 (a) に示す支点外
1とは、三はさみ型110の内孔が異なり、ワイヤーボンデ
ィング部をリードフレームの裏1面に並べている。図3
1(c) に示す支点外の支点付近型は、支点外1に比べて、
支点外1の内孔が異なり、ワイヤーボンディング部をリード
フレームの裏1面に並べている。

それが事實上、図3 (a) に示す天井内、図3 (b) に示す天井内において、手ははの手元からならぬ手を抜けず、電子ビームの面を直接手元として用いていらしのであり、日本二式を採用した結果である。

例にウイヤ220により、インテリード201の声2
面231へひとことはされている。エヌモ2の場合は、
英語の1音節と同様に、ニズミを200と見れば音と
の実的な関係は、モテE203の元音基に進行された
ときはそのニズミからなる英音元233Aを介してプリント
出版家へ送ることにより行かれる。

(00201) 三回、本実験の2のモードは常に、図1 (a)、10 (b) に示す、ダイバードを用たない、シングルによりかねて^{シングル}されたリードフレーム230を用いたもので、その振幅万周に実現¹内とほぼ同じ²であるが、異なる点は、実現¹のときには³モードをインナーリードに固定したせいで⁴ワイヤボンディングを行ない、拘束⁵して⁶いるに拘し、本実験2の場合は、モードは⁷210をインナーリード231とともに⁸実現¹実現²モード⁹上に固定した結果で、ワイヤボンディング二種を行ない、拘束⁵して⁶いるのである。尚、拘束⁵はのプレスによる不規則部分である。モードの名前は、実現¹と同である。図10 (a) に示すリードフレーム230はともには、図9 (a) に示すリードフレーム230とはまたさと¹⁰にしてもある。即ち¹¹、¹²リードフレーム230に示すシングルモードのものは、図10 (a) に示すモードにてもう、この図、図10 (c) (d) に示すように、三本、両端のためモード¹³を260 (ポリイミドビニール) を用する。

(0.6.22) 本日で、実戦的との近接距離が最も適切
を達成し、図 6 (a) は実戦所の近接距離を示す
図の正確度であり、図 6 (b) は図 6 (a) の A-S-A
6 におけるインテーリード界の正確度を示す。図 6 (a)
の 5.5-B 6 におけるインテーリードの正確度であ
る。次、実戦所のエスカレートの内最も実戦的
感じとなる、図には示した。図 6 (c) は実戦所
界、3.10 はエスカレート、3.12 はパンプ、3.30 に
リードフレーム、3.31 はインテーリード、3.31 A は
リードフレーム、3.31 A 6 はエスカレート、3.31 A 5 はエスカ
レート、3.31 A 6 はエスカレート、3.31 にスロモ、3.31 A 6 はエ
スカレート、3.33 B にはエスカレート、3.33 C には上エスカレート、3.4 には

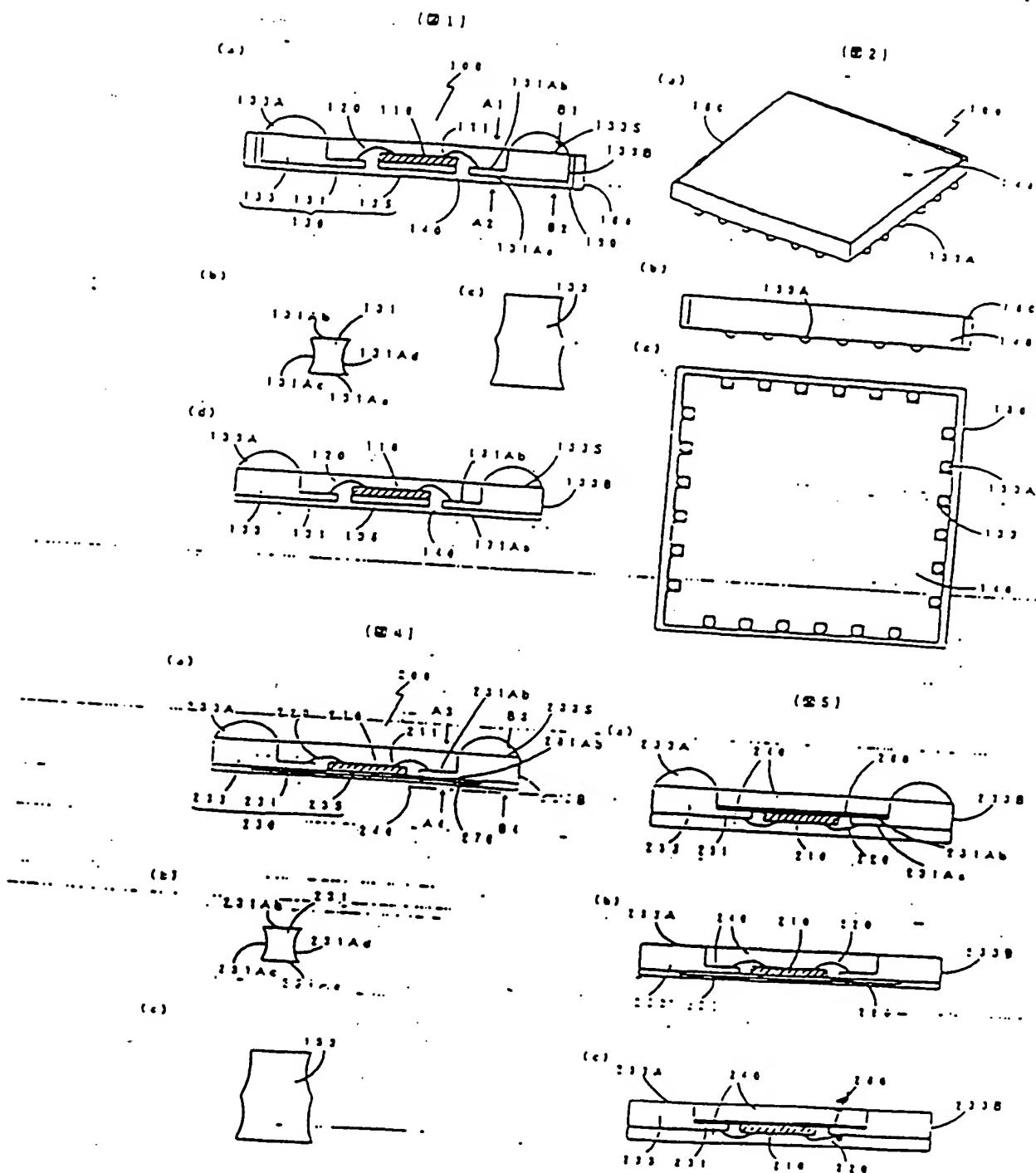
以上是原告、350は高密度テープである。これを右の
のことは右のようにいっては、キスは子コト10に、パン
コト11によりインテリードコト10のW2を2314と
に固定され、次第にインテリードコト10と固定して
いる。リードフレーム330は、図10(a)、610
(b)に示すかのもので、図10に示すニッサンゲル
エにより固定されたものを示している。図10(a)、
(b)に示すように、インテリードコト10のW2を
W1A、W2A(37100μm)ともこの部分の高さを
方向の間のW1Aよりも大きくなってしまおり、更に、イン
テリードコト10のW2を331Aはインテリード
の内側に向かって凹んだ形状で、図10(b)Aに示す
てあることより、インテリードの表面にかかる
とともに、インテリードコト10のW2を331Aに
において、エアエミテとパンプにて次第に充満する
に、図10(c)、(d)のよう位形が美しいものと
ている。また、これを内側の場合は、元気の1や元
2の当をとて内側に、キスは子コト100と固定部との
気の内側は、元気の1と元気の2に受けられたキス
のキスからなるキス子コト10を介してプリント基板
へ固定されることにより行かれる。」

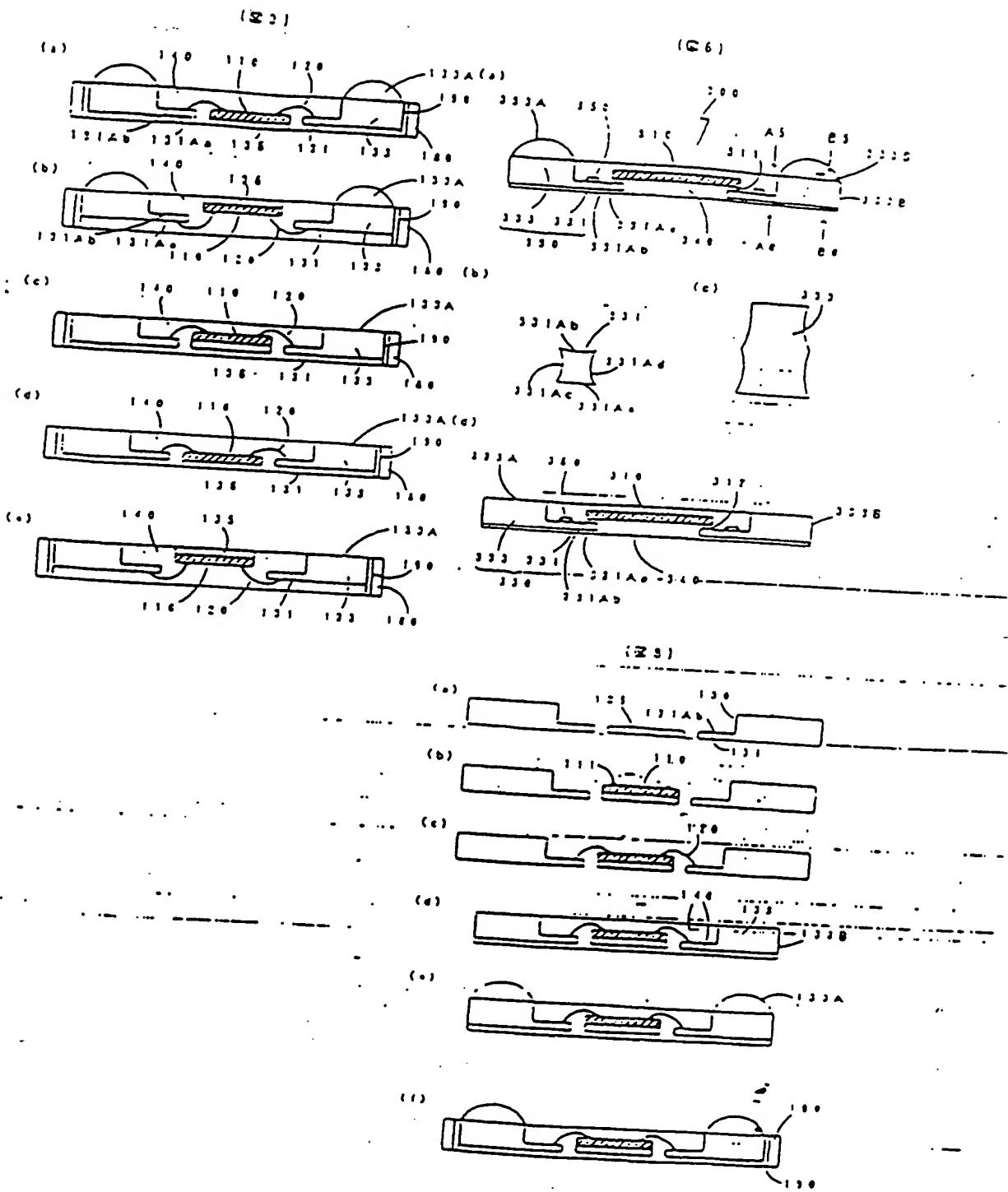
(0023) 天然物のキラリ色に、天然物のキラリ色
キラリ色の生き方に異なり、図12に示すニッティングに
より効果をえたたんニビクレニムを用いたものがある
が、キラリ色の生き方には同じ工法である。
異なる点に、天然物のキラリ色の生き方にキラリ色
モインテリードに匹敵したままでワイヤボンディング
を行い、それが止しているにガレ、天然物のキ
ラリ色の生き方に、キラリ色モインテリードをインテリード
ドコリにパンプを介して匹敵して本物に匹敵した
まで本物に止じている点である。一方、本物に止じた後
によろテテヨリの点、天子の点に、天然物の
キラリ色の生き方に同じである。

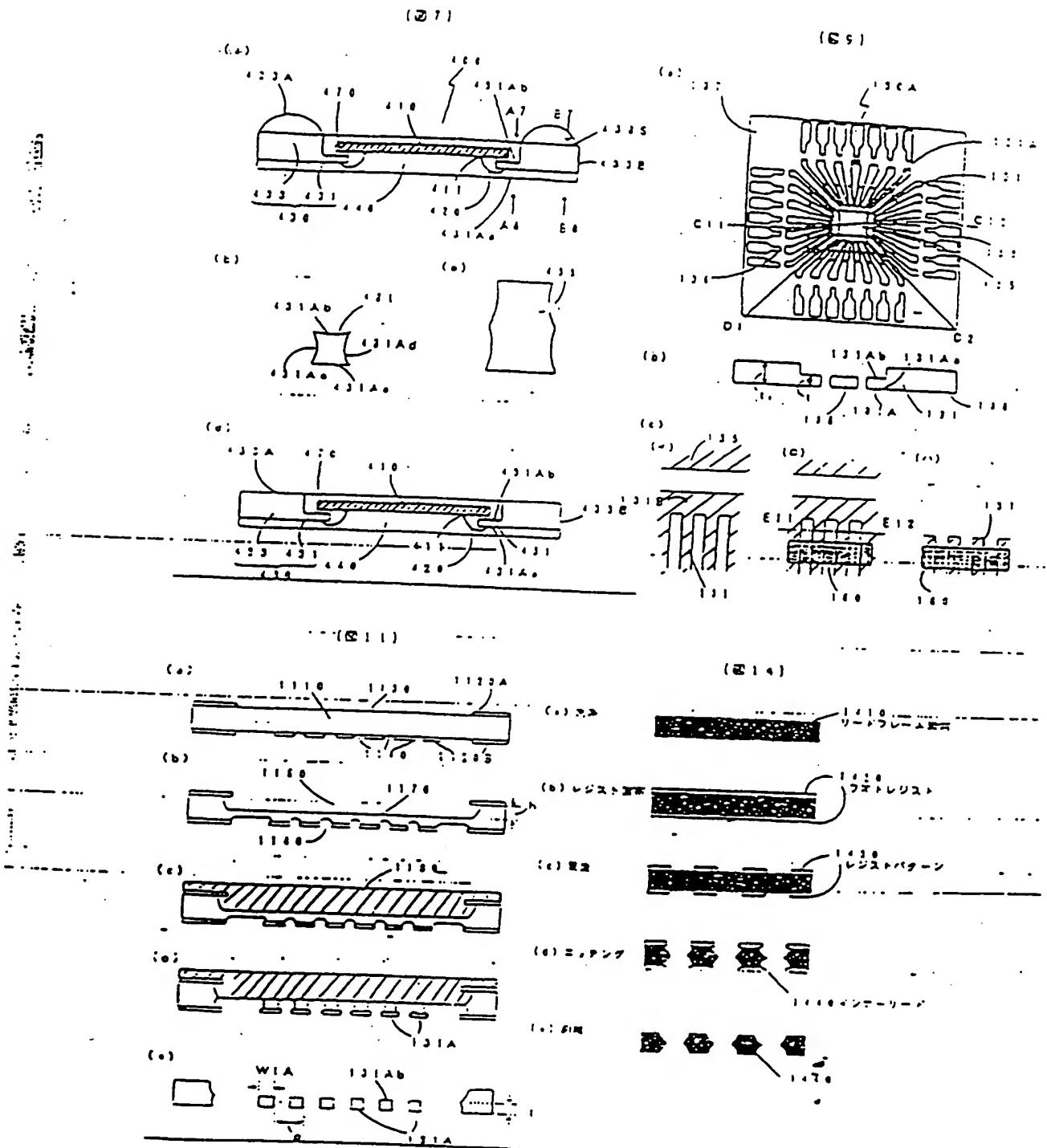
(10024) 区6 (a) は、大阪府内3の市は市立の支
府内市立の支立である。区6 (a) に示す支立

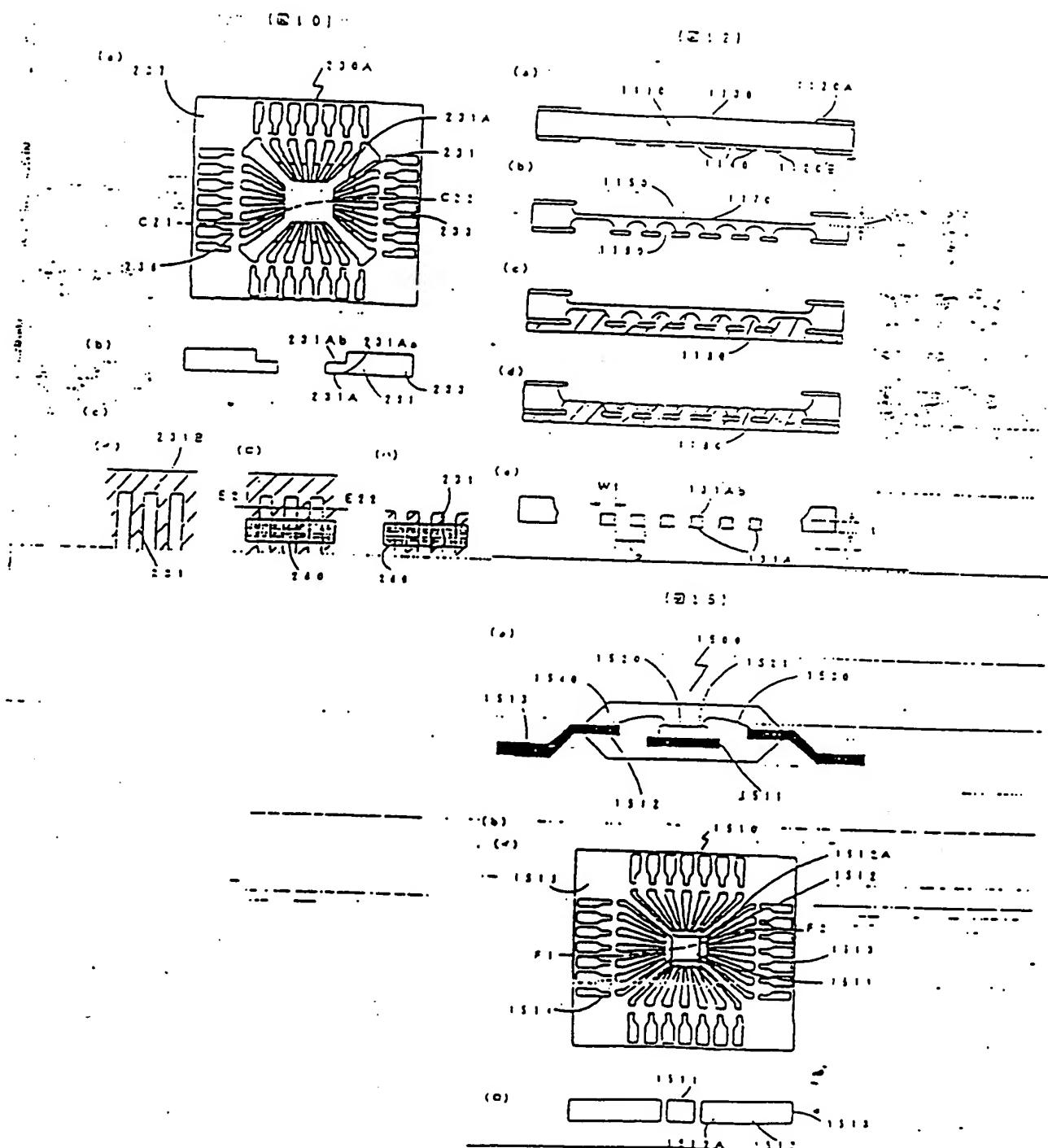
〔10025〕において、高石側の取扱料金を支拂うと
を述べる。図7 (a) は高石側の取扱料金を支拂う
のが西国であり、図7 (b) は図7 (a) のA7-A
8におけるインテリード区の西国で、図6 (c) に
図6 (a) のA7-A8における西千区の西国であ
る。一方、高石側の支拂うる料金を支拂うとば
らばならない。図には示した。図7中、200は支拂

(10)		14459-8205
190	日	ードフレームミガキ
240	日	1331A6
260	日	イニシグロ
270	日	1410
280	日	ードフレームミガキ
350	日	1420
360	日	オトレジスト
470	日	1430
480	日	ジストバターン
1110	日 10	1440
1120A, 1120B	リ	ンナーリード
1130	レ	1510
1の底ニロ	日	ードフレーム
1140	日	1511
2の底ニロ	日	イバード
1150	日	1512
1の凹部	日	ンナーリード
1160	日	1512A
2の凹部	日	ンナーリード元
1170	日	1513
280	日	フターリード
1180	日	1514
ラテング底ニロ	ニ	ルバ-
1320A, 1320C, 1320D	日	1515
1321B, 1321C, 1321D	日 10	レーム部 (右部)
1331B, 1331C, 1331D	日	1521
1331A6	日	底部 (バッド)
	日	1530
	日	1540
	日	止用面









(2 : 2)

